



Universitat d'Alicant
Universidad de Alicante



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Specialized Processor Architectures Lab



**- CIE 2006 Contribution -
'The Role of Algebraic Models
and Type-2 Theory of
Effectivity in Special
Purpose Processor Design'**

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'The Role of Algebraic Models and TTE in Special Purpose Processor Design'

introduction

method

processor
design

conclusions

Contents

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 - problem formalization
 - computability analysis
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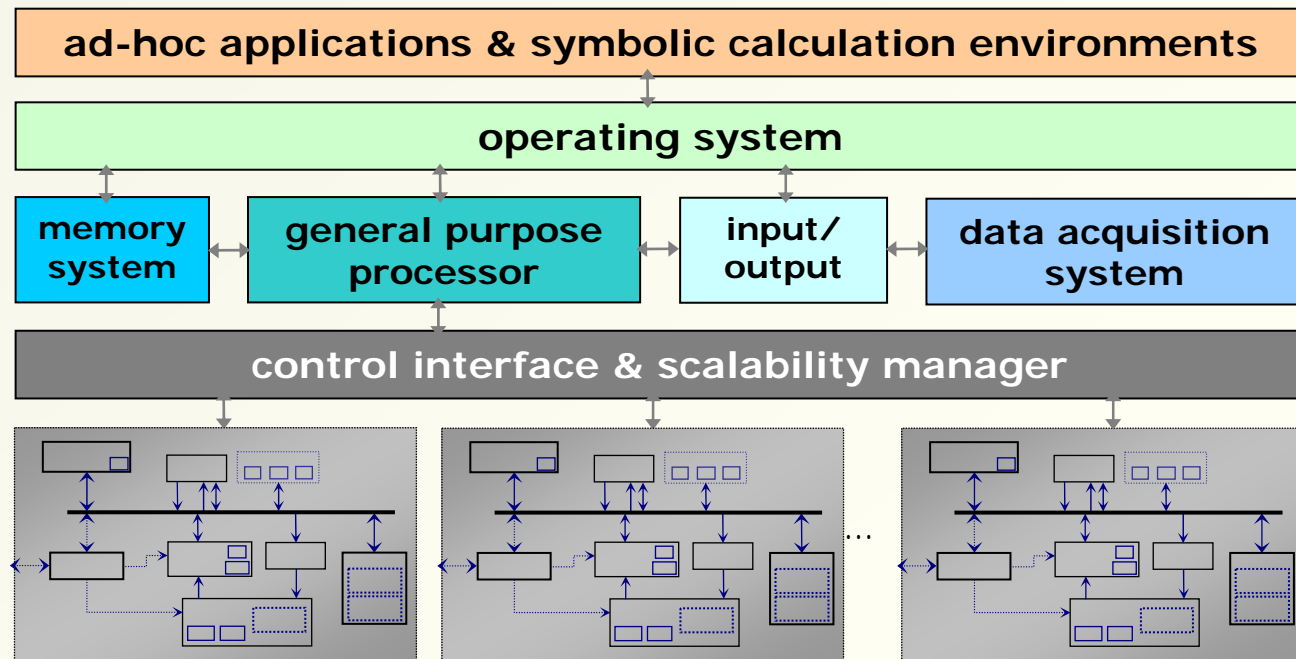
Research Motivation

"special purpose processor for integral transforms"

Specialized Processor Architectures Lab

→ Scientific Computing

Architecture overview



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Background

"feasibility barriers in paradigm application"

- ✚ Scientific Computing
 - reliability demands in computer characterization of complex physical problems
 - ➔ **Computable Analysis**
- ✚ VLSI design
 - correctness in specification and verification of processors
 - ➔ **Formal Methods: Algebraic Models**
- ✚ Computer Arithmetic
 - limited hardware support for arithmetic precision management (IEEE 754)
 - ➔ **signed-digit arithmetic**
- ✚ Technology trends
 - ➔ **hybrid chips (μP + ad-hoc hardware)**
 - ➔ **memory integration improvements**

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Type-2 Theory of Effectivity

- ✚ Provides a coherent bridge between two classical disciplines: analysis/numerical analysis and computability/complexity theory
 - ✚ Presents a realistic model of computation based on Type-2 machines
 - ✚ Provides a concrete computability concept based on naming systems and realizations
 - ✚ Allows the definition of computable functions on the set of all real numbers
 - ✚ Allows a natural complexity theory
- **The representations based on signed-digit notation are feasible for developing ad-hoc hardware arithmetic support (precision criteria)**
- **The amount of memory available limits the feasibility of representation implementation**

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Algebraic Models of Processors

- ✚ Formal paradigm for VLSI design
 - ✚ Allows the isolation some fundamental scientific structural features of processor computation (behavior over time and of data representation and operation)
 - ✚ Specification and verification of computer architecture techniques (microprogramming), and models (pipelined and superscalar processors)
 - ✚ Connection with verification tools such as Maude and HOL
- **Algebraic abstraction support for complex computer architectures**
- **Realistic approach by levels: Programmer & Abstract Circuit**

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Formalization of Requirements

✚ **INPUT:** informal problem description

✚ **OUTPUTS:**

- Mathematical expression. Convolution between Lebesgue integrable functions in $L_1(\mathbb{R})$

$$h(x) = f * g(x) = \int_{\mathbb{R}^d} f(x-y)g(y)dy = \int_{\mathbb{R}^d} f(y)g(x-y)dy$$

- Processor requirements and restrictions

- Support for heterogeneous data sources (symbolic calculation programs and real world data series)
- Support for scalability features by levels of parallelization of the calculation
- Support for variable precision capabilities in order to cover a wide range of precision requirements
- Support for calculation time restrictions and result quality management

- Test scenarios



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Computability Analysis

✚ INPUTS:

- Mathematical expression
- Precision requirements

✚ OUTPUTS:

- Computable representation of convolution operation between Lebesgue integrable functions in $L_1(\mathbb{R})$ spaces
 - rational step functions
 - normalized signed digit notation
- Complexity Analysis



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Specification

✚ INPUTS:

- Requirements and restrictions
- Computable representations and algorithms

✚ **OUTPUT:** Algebraic Specification of the processor

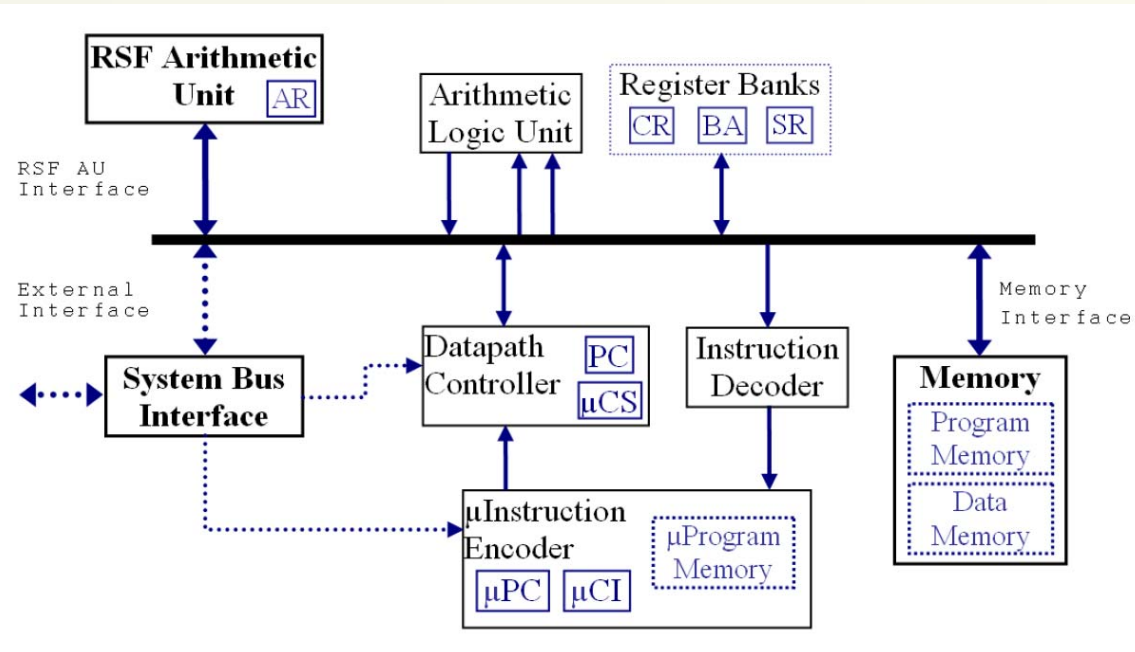
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Functional Specification

✚ Modules



- ✚ Instruction set (Status_Request, Configuration_Request, Configuration_Set, Halt, Convolution)
- ✚ Banks of registers (Configuration, Base-Adress, Status, Arithmetic)



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Algebraic Specification

✚ Programmer's level

- state and next state algebras
- machine algebra
- next state and output function

✚ Abstract circuit level

- program memory
- data memory organization
- rational step function arithmetic unit
- control unit
- state and next state algebras
- machine algebra
- next state and output function

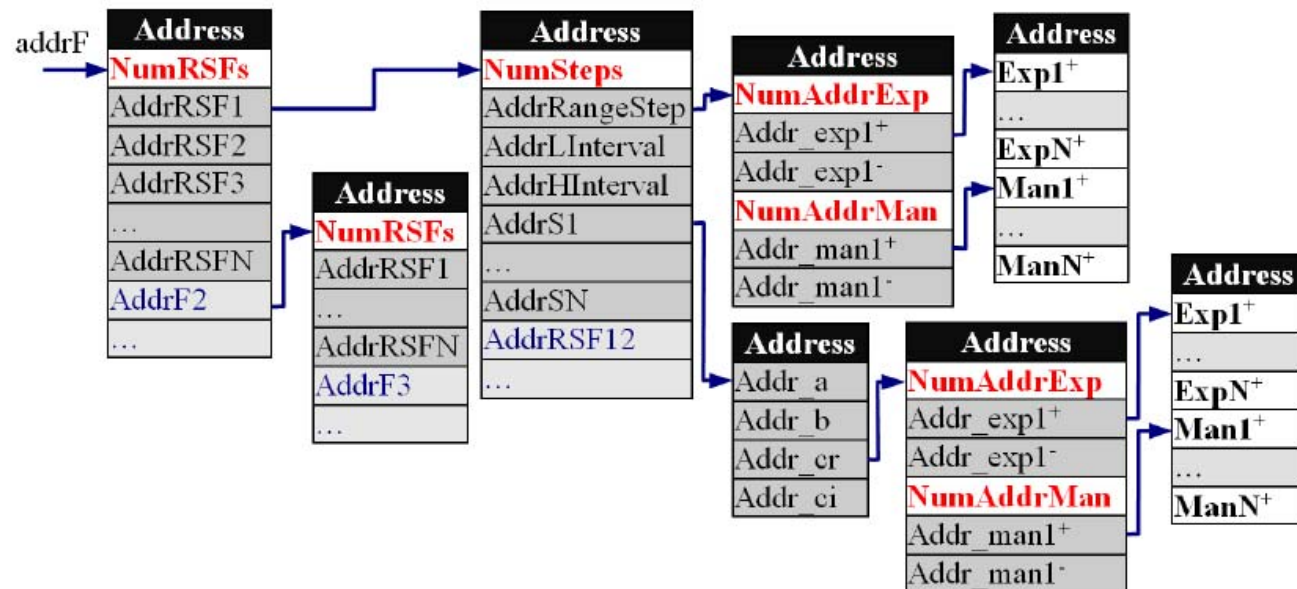
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Algebraic Specification. Data memory organization

- ✚ Mapping functions: $\rho_{head_name}, \rho_{addrF}, \rho_{addrRSF}, \rho_{headStep}, \rho_{addrRangeStep}, \rho_{addrLint}, \rho_{addrHint}, \rho_{addrA}, \rho_{addrB}, \rho_{addrCr}, \rho_{addrCi}, \rho_{RangeStep}, \rho_{IInterval}, \rho_{HInterval}, \rho_a, \rho_b, \rho_{Cr}, \rho_{Ci}$
- ✚ Data memory mapping



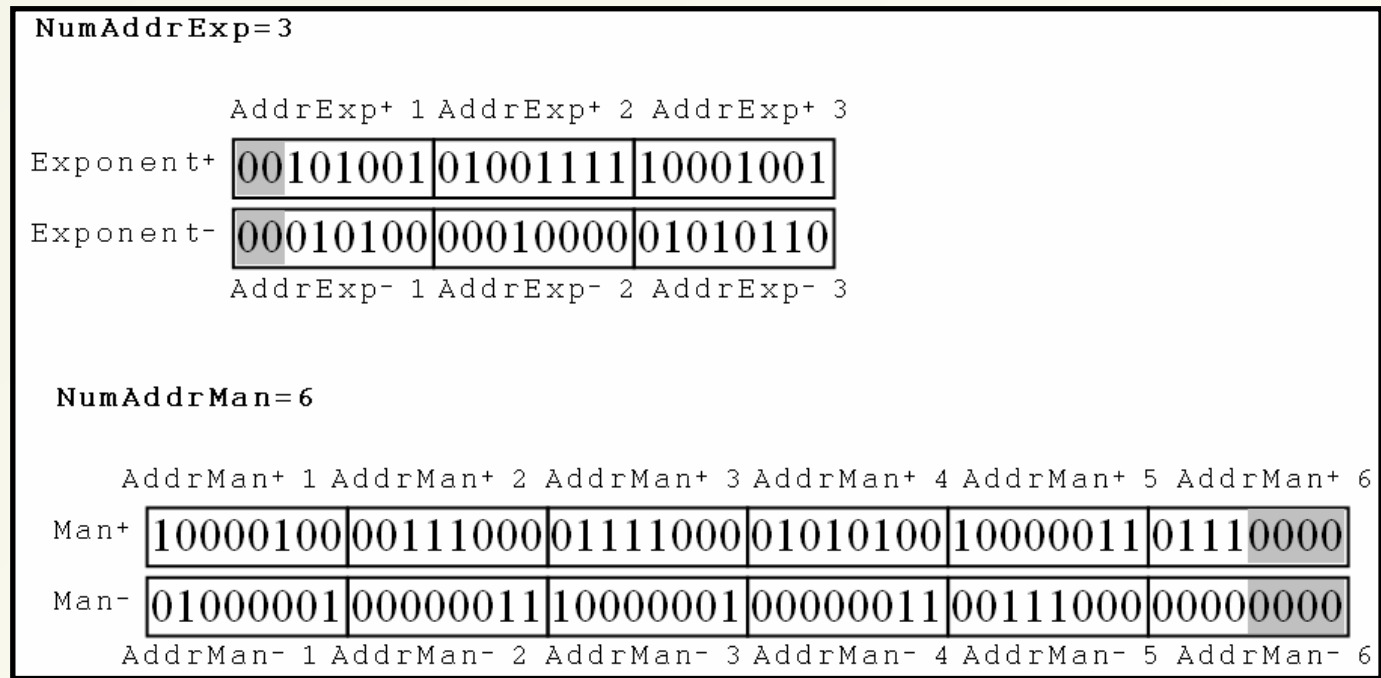
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Algebraic Specification. Data memory storage

✚ Normalized signed-digit representation





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Conclusions

- ✚ Novel theoretical approach for designing a processor for computable scientific computing calculations
 - Type-2 Theory of Effectivity
 - Algebraic Models of Processors
- ✚ Case of study: Convolution between functions $L_1(\mathbb{R})$
- ✚ Research in progress
 - Complete algebraic specification and verification
 - Prototype implementation and performance evaluation



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